

Amendments to the Claims

Please amend claims 1, 5 and 9, and add new claims 10 and 11 as shown in the following list of claims. This listing of claims will replace all prior versions, 5 and listings, of claims in the application.

- 1 1. (currently amended) A data carrier, which is designed to modulate a carrier signal that can be received in a contactless manner, and which is equipped with transmission means, designed to transmit the carrier signal, and which is equipped with an electrical circuit, which circuit is equipped with at least one terminal, to which terminal the transmission means is connected and via which terminal the carrier signal can be fed to the circuit, and which circuit is equipped with a data signal source designed to generate and emit a data signal, and which circuit is equipped with modulation means designed to receive the data signal and, using the data signal, to modulate the carrier signal occurring at the at least one terminal, and to generate an amplitude-modulated signal, in which amplitude-modulated signal ~~signal~~ edges occur, characterized in that signal-edge influencing means provided, which is designed to influence the slope characteristic of the signal edges in the amplitude-modulated signal.
- 1 2. (previously amended) A data carrier as claimed in claim 1, characterized in that the signal-edge influencing means is realized by filtration means.
- 1 3. (previously amended) A data carrier as claimed in claim 2, characterized in that the filtration means is provided between the data signal source and the modulation means and designed to filter the data signal that can be emitted from the data signal source to the modulation means.
- 1 4. (previously amended) A data carrier as claimed in claim 2, characterized in that the filtration means is formed by a low-pass filter.

1 5. (currently amended) A circuit for a data carrier which is designed to
2 modulate a carrier signal that can be received in a contactless manner, and which
3 is equipped with transmission means to transmit the carrier signal, which circuit is
4 equipped with at least one terminal, to which terminal the transmission means can
5 be connected, and via which terminal the carrier signal can be fed to the circuit,
6 and which circuit is equipped with a data signal source designed to generate and
7 emit a data signal, and which circuit is equipped with modulation means designed
8 to receive the data signal and, using the data signal, to modulate the carrier signal
9 occurring at the at least one terminal, and to generate an amplitude-modulated
10 signal, in which amplitude-modulated signal ~~signal~~ edges occur, characterized in
11 that signal-edge influencing means is provided, which is designed to influence the
12 slope characteristic of the signal edges in the amplitude-modulated signal.

1 6. (previously amended) A circuit as claimed in claim 5, characterized in that
2 the signal-edge influencing means is realized by filtration means.

1 7. (previously amended) A circuit as claimed in claim 6, characterized in that
2 the filtration means is provided between the data signal source and the modulation
3 means and designed to filter the data signal that can be emitted from the data
4 signal source to the modulation means.

1 8. (previously amended) A circuit as claimed in claim 6, characterized in that
2 the filtration means is formed by a low-pass filter.

1 9. (currently amended) A circuit as claimed in claim 5 4, characterized in that
2 the circuit is realized as an integrated circuit.

1 10. (new) A circuit as claimed in claim 5, characterized in that the modulation
2 means includes a transistor with a control terminal, and the signal-edge
3 influencing means includes a resistor connected to the control terminal of the
4 transistor and a capacitor connected to the control terminal of the transistor and
5 ground.

1 11. (new) A data carrier as claimed in claim 1, characterized in that the
2 modulation means includes a transistor with a control terminal, and the signal-
3 edge influencing means includes a resistor connected to the control terminal of the
4 transistor and a capacitor connected to the control terminal of the transistor and
5 ground.